AMENDMENTS TO THE CLAIMS

1. (currently amended) A control method for controlling a data processing system including a logic circuit region where circuits are dynamically reconfigurable, the control method comprising:

~~a step of~~ obtaining an architecture code, the architecture code including object circuit information for mapping an object circuit that is at least part of a circuit for executing an application onto part of the logic circuit region, interface circuit information for mapping an interface circuit in contact with the object circuit onto the logic circuit region, and boundary condition to be realized in the interface circuit;

~~a step of~~ mapping the object circuit and the interface circuit in contact with the object circuit onto the logic circuit region according to the object circuit information and the interface circuit information of the architecture code; and

~~an~~ activating ~~step of controlling~~ the interface circuit based on the boundary condition of the architecture code, and

wherein the object circuit is a divided circuit of a hardware module for implementing a function, and wherein the boundary condition includes information of timing control of data supplying to the object circuit so that the object circuit functions as the divided circuit of the hardware module when the object circuit is mapped spatially and/or temporally divided to other divided circuits.

2. (cancelled)

3. (cancelled)

4. (currently amended) The control method according to Claim 1, wherein the ~~step of~~ mapping includes, when the interface circuit information and the boundary condition match or correspond that of an adjacent object circuit at a boundary, mapping the object circuit connecting with the adjacent object circuit without passing respective interface circuits.

5. (currently amended) The control method according to Claim 1, wherein the activating ~~step~~ includes reflecting a state of an interface circuit of another object circuit mapped by spatially and/or temporally dividing on the logic circuit region in control of the interface circuit of the object circuit based on the boundary condition.

6. (currently amended) The control method according to Claim 1, wherein the ~~step of~~ obtaining includes selecting the architecture code to be obtained based on information of behavioral environment including a request to the data processing system, an execution state of mapped object circuit, and a usable state of the logic circuit region.

7. (currently amended) The control method according to Claim 1, wherein the ~~step of~~ obtaining includes obtaining the architecture code via a communication network.

8. (original) The control method according to Claim 1, wherein the logic circuit region includes a plurality of circuit blocks constructed of a predetermined number of reconfigurable elements and the architecture code includes the object circuit information in units of the circuit blocks.

9. (currently amended) A data processing system comprising:

a logic circuit region where circuits are dynamically reconfigurable;

a load unit for obtaining an architecture code, the architecture code including object circuit information for mapping an object circuit that is at least part of a circuit for executing an application onto part of the logic circuit region, interface circuit information for mapping an interface circuit in contact with the object circuit onto the logic circuit region, and boundary condition to be realized in the interface circuit;

a mapping unit for mapping the object circuit and the interface circuit in contact with the object circuit onto the logic circuit region according to the object circuit information and the interface circuit information of the architecture code, and

a behavior control unit for controlling the interface circuit according to the boundary condition of the architecture code, and

wherein the object circuit is a divided circuit of a hardware module for implementing a function, and wherein the boundary condition includes information of timing control of data supplying to the object circuit so that the object circuit functions as the divided circuit of the hardware module when the object circuit is mapped spatially and/or temporally divided to other divided circuits.

10. (cancelled)

11. (currently amended) The data processing system according to Claim 9~~10~~, wherein the load unit, the mapping unit, and the behavior control unit are hardware modules and are implemented in the logic circuit region as divided circuits.

12. (original) The data processing system according to Claim 9, wherein the mapping unit carries out mapping of the object circuit and the interface circuit onto any usable region in the logic circuit region.

13. (original) The data processing system according to Claim 9, wherein when the interface circuit information and boundary condition match or correspond that of an adjacent object circuit at a boundary, the mapping unit carries out mapping of the object circuit connecting with the adjacent object circuit without passing respective interface circuits.

14. (original) The data processing system according to Claim 9, wherein the behavior control unit reflects a state of an interface circuit of another object circuit mapped by spatially and/or temporally dividing on the logic circuit region in control of the interface circuit of the object circuit based on the boundary condition.

15. (original) The data processing system according to Claim 9, further comprising a boundary information memory for storing a state of an interface circuit of an object circuit mapped by spatially and/or temporally dividing on the logic circuit region.

16. (original) The data processing system according to Claim 9, wherein the load unit obtains the architecture code from an architecture library including a plurality of architecture codes, based on information of behavioral environment including a request to the data processing system, an execution state of mapped object circuit, and a usable state of the logic circuit region.

17. (original) The data processing system according to Claim 9, wherein the load unit obtains the architecture code via a communication network.

18. (currently amended) The data processing system according to Claim 9~~10~~, further comprising an architecture library including a plurality of architecture codes for configuring a plurality of hardware modules.

19. (original) The data processing system according to Claim 9, wherein the logic circuit region includes a plurality of circuit blocks constructed of a predetermined number of reconfigurable elements and the architecture code includes the object circuit information in units of the circuit blocks.

20. (original) The data processing system according to Claim 19, wherein the elements respectively include:

n inputs and n outputs, the n being a plural;

an input interface for freely selecting input data out of the n inputs;

an operation core for performing a logic operation on the input data selected by the input interface and outputs output data, wherein the logic operation is changeable;

an output interface for freely selecting output from at least one of the n inputs and the output data and outputs the output via at least one out of the n outputs.

21. (original) The data processing system according to Claim 20, wherein the operation core includes a selector into which a multibit function code that designates logic operation is inputted and which selects the output data according to the input data.

22. (original) The data processing system according to Claim 20, wherein the operation core includes a register for latching one of data of one of the n inputs and the output data.

23. (currently amended) An automated control system comprising:

a data processing system according to Claim 9 ~~10~~; and

a plurality of automated control mechanisms for which at least one of a plurality of hardware modules to be configured in the data processing system is used in respective control or data processing,

wherein mapping of divided circuits of the plurality of hardware modules are dynamically performed in the logic circuit region.

24. (original) The automated control system according to Claim 23, further including a communication mechanism for obtaining the architecture code by communication with outside.

25. (original) A terminal comprising:

a data processing system according to Claim 9; and

a communication mechanism for obtaining the architecture code by communication with outside.

26. (currently amended) A recording medium on which architecture code for controlling a data processing system including a logic circuit region where circuits are dynamically reconfigurable is recorded, the architecture code including object circuit information for mapping an object circuit that is at least part of a circuit for executing an application onto part of the logic circuit region, interface circuit information for mapping an interface circuit in contact with the object circuit onto the logic circuit region, and boundary condition to be realized in the interface circuit, and

wherein the object circuit is a divided circuit of a hardware module for implementing a function, and wherein the boundary condition includes information of timing control of data supplying to the object circuit so that the object circuit functions as the divided circuit of the hardware module when the object circuit is mapped spatially and/or temporally divided to other divided circuits.

27. (cancelled)

28. (currently amended) A method for generating an architecture code for controlling a data processing system including a logic circuit region where circuits are dynamically reconfigurable, the architecture code including object circuit information for mapping an object circuit that is at least part of a circuit for executing an application onto part of the logic circuit region, interface circuit information for mapping an interface circuit in contact with the object circuit onto the logic circuit region, and boundary condition to be realized in the interface circuit, the method comprising:

~~a step of~~ generating object circuit information by dividing a netlist of the circuit for executing the application and resolving place and route issues within divided ranges of the netlist;

~~a step of~~ generating interface circuit information from information in the netlist for forming boundary of the object circuit configured by the object circuit information; and

~~a step of~~ converting the netlist into a group of object circuits, resolving place and route issues among the object circuits, and generating boundary condition of interface circuits of respective object circuits, and

wherein the object circuit is a divided circuit of a hardware module for implementing a function, and wherein the boundary condition includes information of timing control of data supplying to the object circuit so that the object circuit functions as the divided circuit of the hardware module when the object circuit is mapped spatially and/or temporally divided to other divided circuits.

29. (cancelled)

30. (currently amended) A data processing system including a logic circuit region where circuits are dynamically reconfigurable,

wherein the logic circuit region includes elements that are reconfigurable, and

the elements respectively include an operation core that performs a logic operation on input data and outputs output data, the operation core including a selector into which a multibit function code for designating the logic operation is inputted and which selects the output data according to the input data as a logic operation element.

31. (original) The data processing system according to Claim 30, wherein the elements respectively include:

n inputs and n outputs, the n being a plural;

an input interface that selects the input data out of the n inputs; and

an output interface that selects output from at least one of the n inputs and the output data and outputs the output via at least one out of the n outputs.

32. (original) The data processing system according to Claim 30, wherein the elements respectively include:

four input routes and four output routes,

an input interface that freely selects the input data out of the four input routes; and

an output interface that is capable of freely selecting output from the four input routes and the output data and connecting the output to the four output routes.

33. (original) The data processing system according to Claim 31, wherein the operation core includes a register for latching data of at least one of the n inputs or the output data.

34. (original) The data processing system according to Claim 30, further comprising a plurality of circuit blocks constructed of a predetermined number of the elements respectively.